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SYCLOPS

Scaling extreme analYtics with Cross-architecture acceLeration based on OPen Standards

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Cti
Commission des Titres d'Ingénieur

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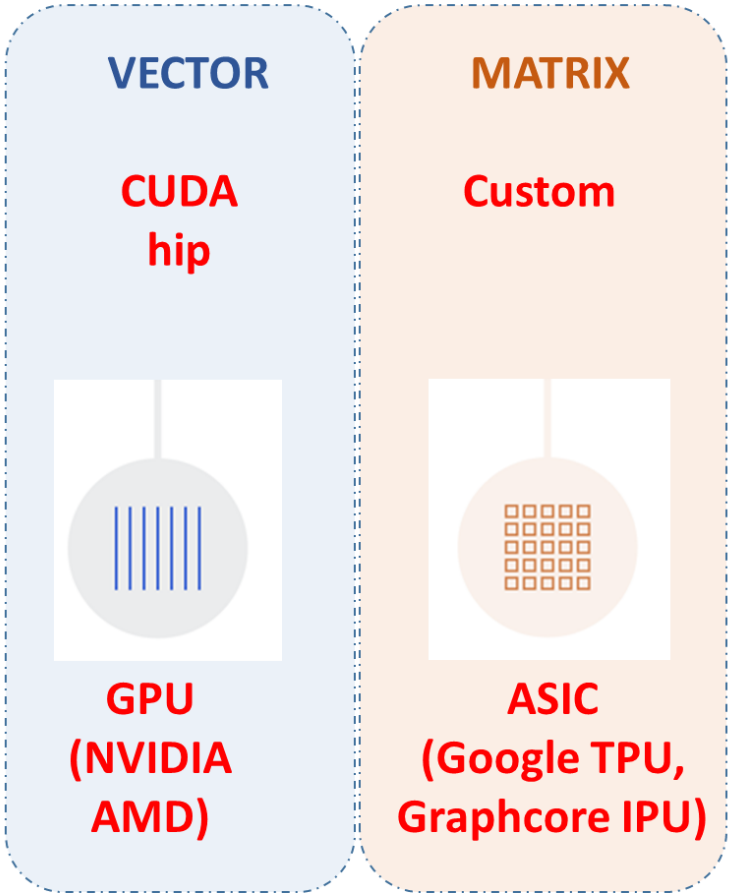
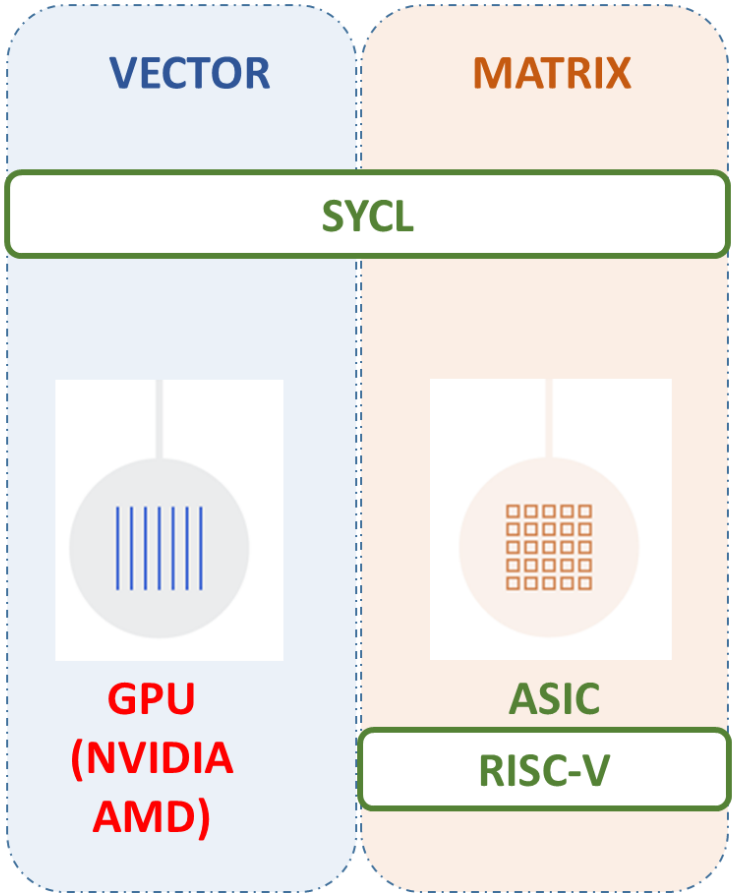
Vision

NON-PORTABLE, PROPRIETARY STACKS



STANDARDS-BASED, PORTABLE SYCLOPS STACK



Democratizing AI acceleration using open standards

Opportunities & Challenges

- **RISC-V vector extensions gaining momentum in AI acceleration**
  - Implementation and verification of RVV accelerators is largely a manual approach
- **SYCL gaining momentum as an open programming model that supports a cross-vendor, cross-architecture computation offloading**
  - SYCL RISC-V compiler backends still immature in supporting RVV
  - SYCL runtimes lack support for efficient scheduling (e.g graph runtime)
  - No SYCL interpreter available today that can enable ad-hoc, interactive data analytics
- **Optimized SYCL libraries (like oneDNN, SYCL-DNN) can boost adoption of open hardware acceleration**
  - SYCL libraries and performance profiling tools are very limited

Project SYCLOPS

- **EC-funded 3-year Horizon Europe project**
- **4 SMEs**
  - ***Codasip (CZ)***: Founding members of RISC-V foundation
  - ***Codeplay (UK):*** Governing members of SYCL standardization
  - ***HIRO (NL)***: Energy-efficient microdatacenters
  - ***ACCELOM (FR):*** AI for integrated genomics (Allied with India's largest biobank)
- **4 Research Institutes/Universities**
  - ***UHEI (GE)***
  - ***CERN (CH)***
  - ***INESC-ID (PT)***
  - ***EURECOM (FR)***

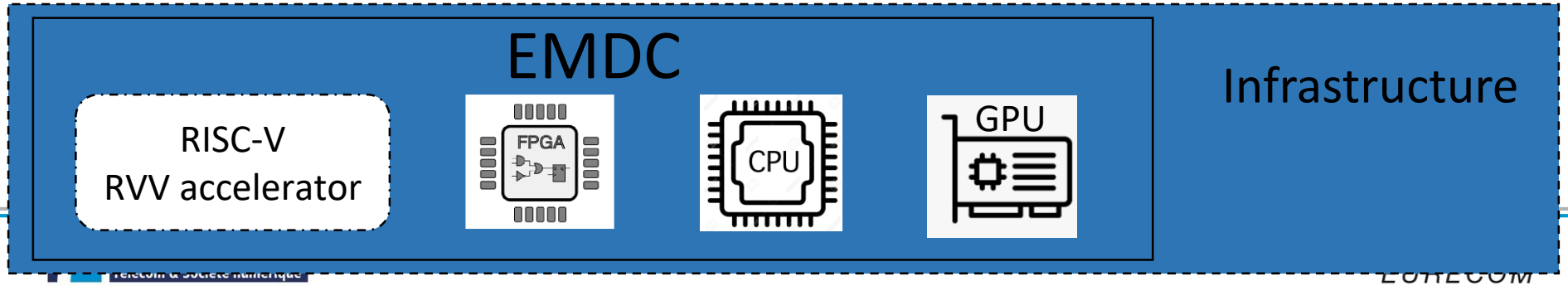
European SMEs at the forefront of AI acceleration

SYCLOPS Stack: Infrastructure Layer

- **RISC-V vector extensions (RVV) gaining momentum in AI acceleration**
  - Implementation and verification of RVV accelerators is largely a manual approach

- Autogenerating HDK, SDK with codAL
- Customizing RVV accelerators with Codasip Studio

- Energy-efficient micro datacenter (EMDC) design based on PCIe5 and CXL
- Customizable, modular packaging for heterogeneous hardware accelerators



SYCLOPS Stack: Platform Layer

- **SYCL gaining momentum as an open, cross-architecture programming model**
  - SYCL RISC-V compiler backends still immature in supporting RVV
  - SYCL runtimes lack support for efficient, cross-processor scheduling
  - No SYCL interpreter available today that can enable ad-hoc, interactive data analytics.

codeplay

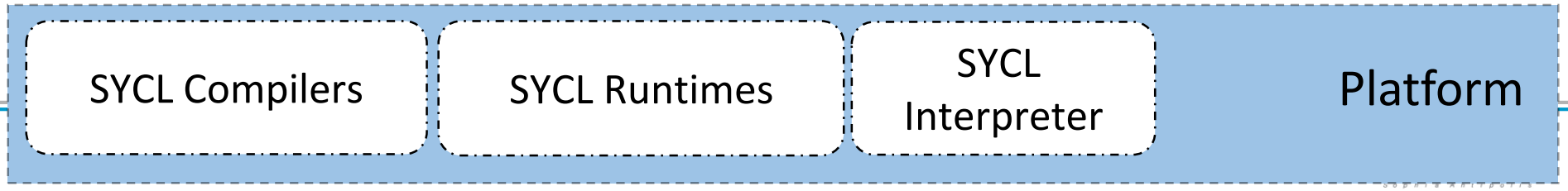
UNIVERSITÄT HEIDELBERG ZUKUNFT SEIT 1386

CERN

- DPCPP support for RVV using oneAPI construction kit
- Optimized runtime to enable computational offloading to RVV accelerators

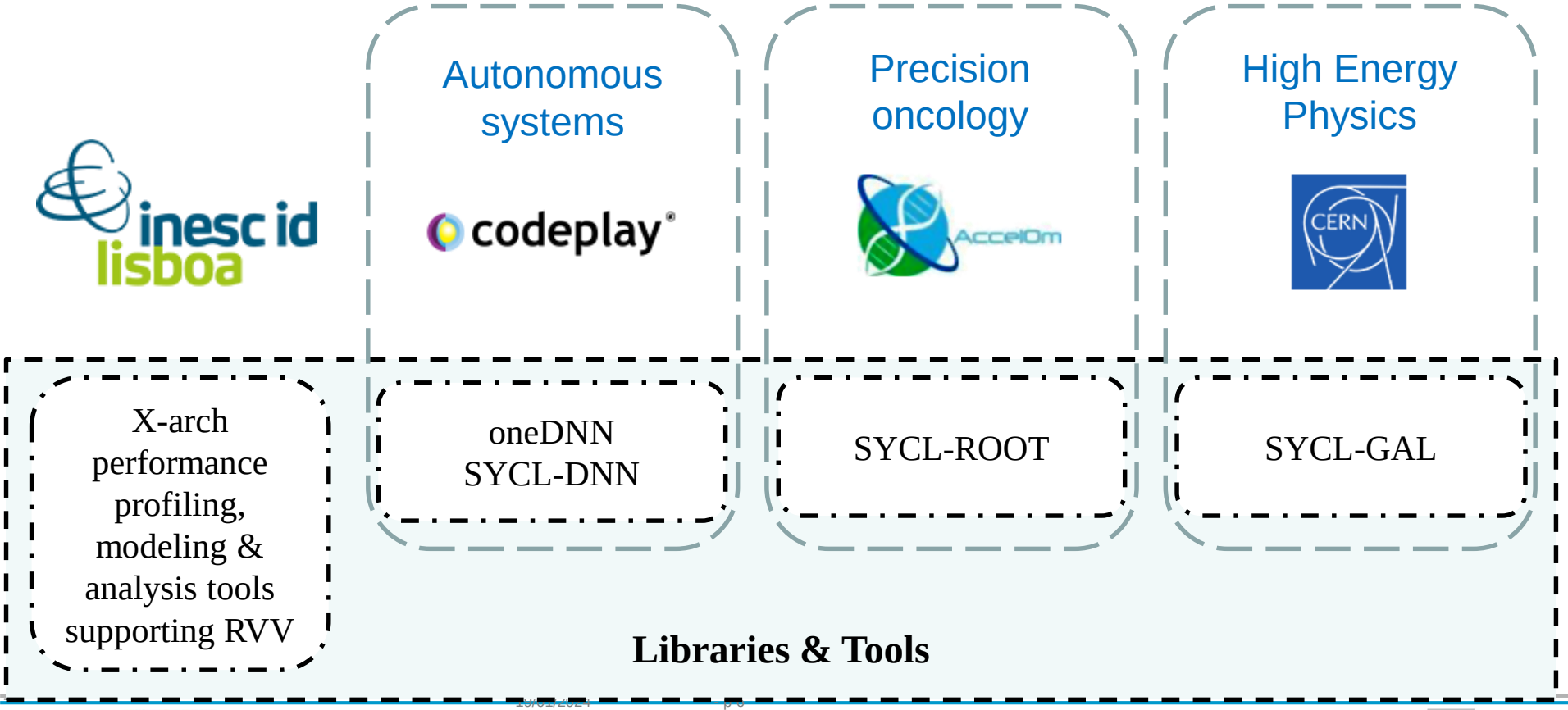
- Optimized hipSYCL/openSYCL support for RVV
- Investigate multi-device scheduling with optimized graph runtime

- Cling—C++ interpreter used in interactive exploration of 1EB of High-Energy Physics data
- Extend Cling to natively support SYCL

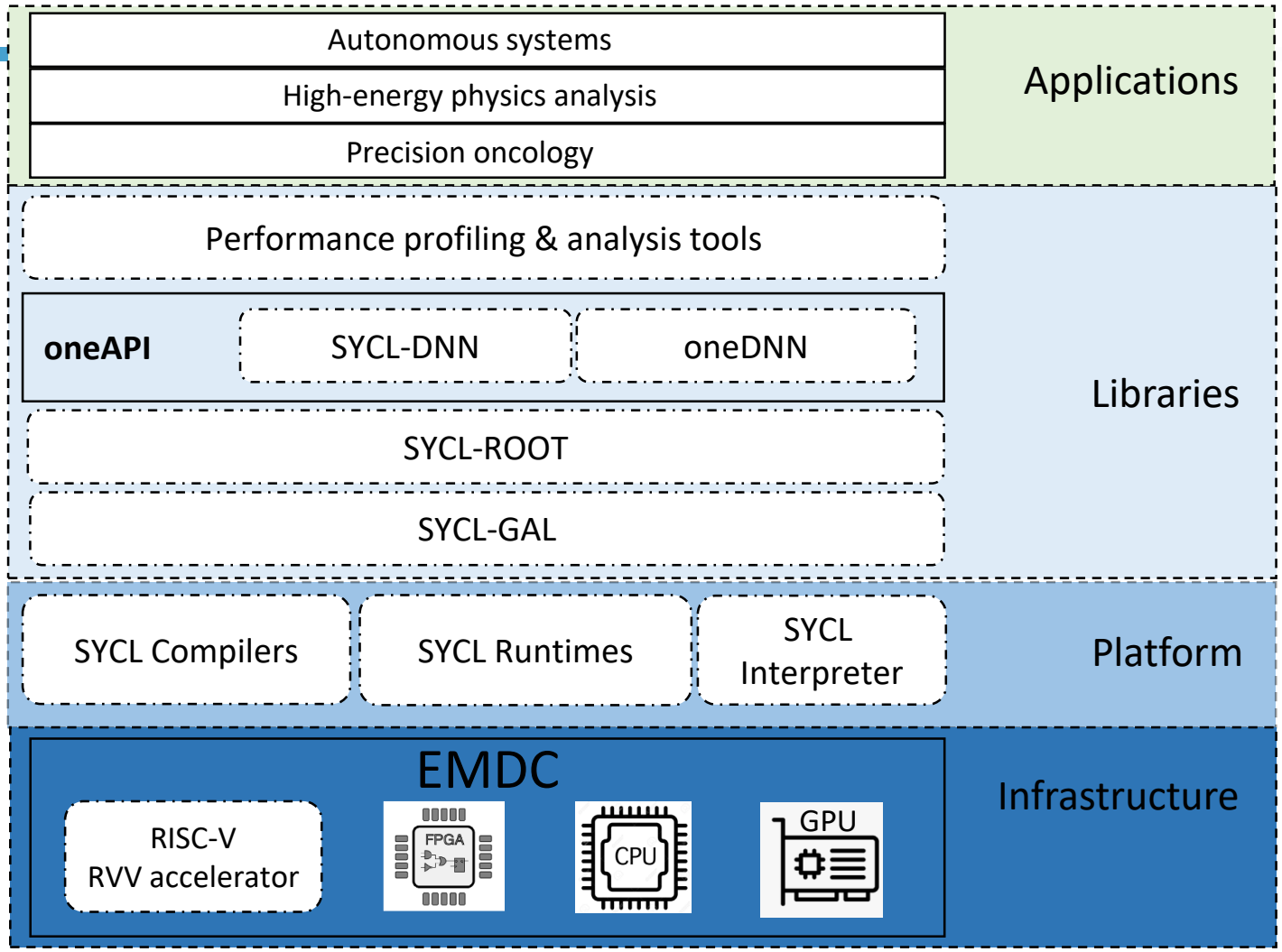


SYCLOPS Stack: Libraries Layer

- **Optimized SYCL libraries (like oneDNN, SYCL-DNN) can boost adoption of open hardware acceleration**
  - SYCL libraries and performance profiling tools are very limited



SYCLOPS Stack: Putting It All Together



SYCLOPS stack will provide open, standards-based acceleration for key verticals

Please reach out for collaboration

https://www.syclops.org/