FLEXIBLE FRONT-END PROCESSING FOR SOFTWARE DEFINED RADIO APPLICATIONS USING APPLICATION SPECIFIC INSTRUCTION-SET PROCESSORS

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ABSTRACT

High computational demands of today's wireless communication standards require the design of highly flexible Software Defined Radio (SDR) platforms like the OpenAirInterface ExpressMIMO platform. A DSP engine of major importance is the Front-End Processor (FEP) which deals with the different air-interface operations at the transceiver side. In this paper we propose an Application Specific Instruction-Set Processor (ASIP) architecture for front-end processing and compare it to a programmable DSP engine as well as to other ASIP solutions. For design comparison we mainly focus on architectural differences and the runtime performance in terms of processing time. The synthesis results are provided for different target technologies.[1]

Index Terms— SDR, ASIP, flexible HW platform

1. INTRODUCTION

Recently, we have witnessed a significant change in the use of mobile phones and other mobile devices. A few years ago these devices focused solely on providing voice communication. In contrast, today's smartphones support a wide range of applications and high data-rate access becomes of major importance. In addition, the requirements of different applications and the variable environment requests the support of multiple wireless communication standards. For example, available smartphones typically include GSM, 3GPP UMTS, WLAN 802.11a/b/g, Bluetooth and most likely LTE in the near future. It is expected that this number increases due to upcoming standards like LTE Advanced and WiMAX, while at the same time updates of existing standards need to be supported as well.

The high computational demands of such wireless communication standards, especially in the physical layer, have commonly been answered by a dedicated subsystem per standard. To allow the execution of the different modes of the given standard, each of them has been implemented by a set of configurable hardware accelerators. By nature, these systems have limited flexibility and can mostly support only the standards they were intended for. Therefore, changes in existing standard specifications or the implementation of new standards require a time-consuming and costly redesign of the hardware architecture. These issues have given birth to the concept of Software Defined Radio (SDR). Key idea is to provide a flexible SDR platform that can support multiple wireless communication standards in a multimodal fashion. Unfortunately, adding flexibility to a hardware design usually comes with the cost of increased area, increased energy consumption and/or reduced computational performance. Earlier investigations [1] have illustrated that a large amount of computational complexity can be efficiently implemented by a vector processing unit and SIMD (Single Instruction Multiple Data) instructions. This paradigm is also visible in recently released SDR platforms in commercial products like Femtocells from TI [2] and Freescale [3], as well as in SDR platforms from academia [4]. In contrast to these solutions, the baseband processing of the OpenAirInterface ExpressMIMO platform [5] is split over several independent subsystems, as depicted in Fig. 1.

In this paper we focus on the design of a flexible Front-End Processor (FEP) for the ExpressMIMO platform. For this purpose, a thorough comparison between a programmable tool-based Application Specific Instruction-Set Processor (ASIP) denoted as the *A-FEP*, a previously designed programmable DSP engine (the *Custom* FEP (C-FEP)) and two other ASIP solutions from academia ([6], [7]) is carried out.

For our ASIP design we used the Language for Instruction-Set Architectures (LISA) [8] which has gained commercial acceptance over the last years. Like the C-FEP, the A-FEP achieves the required real time requirements of latest wireless communication standards when executing the front-end processing part of the physical layer.

The paper is structured as follows: after presenting the related work in Section 3 and a brief introduction of the un-

[1]The research work leading to this paper has been supported by the European FP7 project ACROPOLIS (Advanced coexistence technologies for radio optimization and unlicensed spectrum)

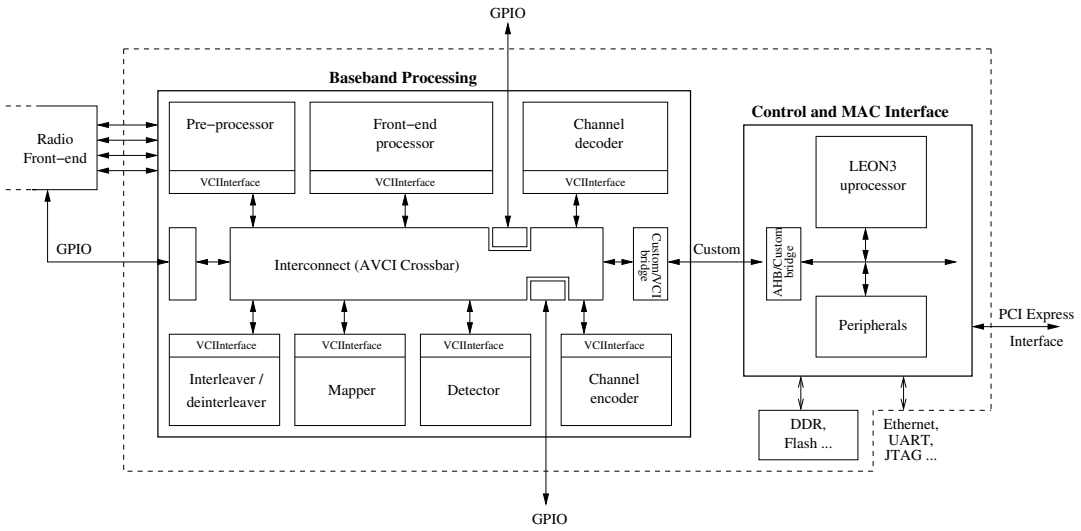

Fig. 1. OpenAirInterface ExpressMIMO Platform - System Overview

derlying front-end processing algorithms and the functional specification of the A-FEP in Section 4.1, the architecture of the A-FEP is enhanced in Section 4.2. Usually, architectures are evaluated in terms of frequency, area, power consumption and the number millions of operations or instructions per second. As the latter does not provide clear information about the processing time of different operations executed on ASIPs, we will provide processing time results based on the actual amount of cycles instead. Two recent academic solutions providing this information are the ones developed by ETH Zürich [7] and by the Cairo University [6]. In Section 3, details of their architectures are provided before we finally present the results of the runtime comparison in Section 5.

2. SYSTEM OVERVIEW

The ExpressMIMO platform is a flexible open-source SDR platform that supports a wide range of different wireless communication standards. To simplify upgrades to future ones like LTE the baseband processing implemented on a Xilinx Virtex 5 LX330 FPGA is split over different independent programmable DSP engines that are connected via a generic Advanced Virtual Component Interface (AVCI) crossbar [9]. The platform further embeds a SPARC LEON3 processor from Gaisler - Aeroflex [10] as main CPU which runs on a Xilinx Virtex 5 LX110 FPGA. The chosen Operating System (OS) is MutekH [11] whose flat function call convention, flat registers and simplified interrupt handling reduce the latencies significantly when compared to other OS like eCos or RTEMs. The design of each DSP engine on the baseband FPGA follows the general structure shown in Fig. 2. This standardized DSP shell is composed of a Control Sub-System (CSS), a DMA engine, a Processing Unit (PU) and a Memory Sub-System (MSS). MSS and PU are custom defined and depend on the functionality of the DSP. Currently all DSP engines are controlled by the main CPU which results in a centralized control flow on the platform. To decrease the resulting communication overhead, an 8 bit micro-controller (UC) coming with a 2 kB data memory can be included in the DSP shell to enable a distributed control flow. During our ongoing work we experienced, that for standards operating on small vector lengths like IEEE 802.11a the communication overhead leads to a significant performance drop. Therefore we decided to extend the functionality of the A-FEP by a set of General Purpose (GP) instructions to overcome this drawback. The UC can still be kept in the design but only for the programming of the DMA engine.

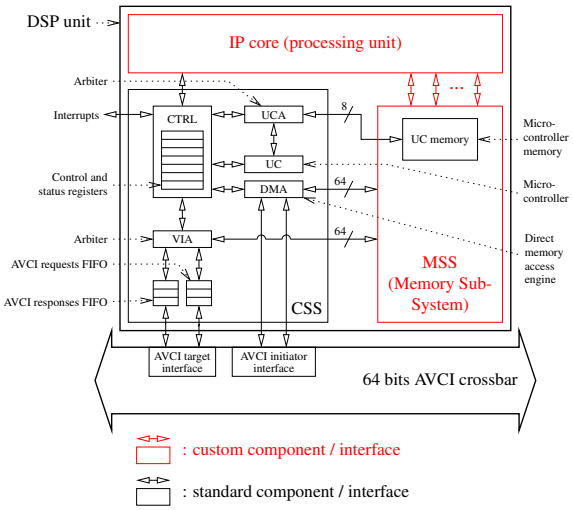

Fig. 2. Standardized DSP shell

3. RELATED WORK

In the context of SDR platforms, one promising design solution are ASIPs that can be seen as a class of microprocessors coming with a specialized Instruction-Set Architecture (ISA). For SDR platform design, ASIPs tend to be suitable candidates as they are meant to fill in the gap between General Purpose Processors (GPPs) and Application Specific Integrated Circuits (ASICs) [12]. Being tailored to a specific application, ASIPs exhibit a lower energy consumption than GPPs or Digital Signal Processors (DSPs) while offering a higher flexibility than ASICs at the same time. During the past years, different solutions for front-end processing ASIPs have been proposed. Some of the architectures focus only on some air-interface algorithms like packet synchronization or channel estimation (e.g. [13]) while other designs are tailored to the processing of a specific group of standards. One example is [14] where the proposed ASIP solution supports the execution of the IEEE 802.15.4a standard only. Instead, the A-FEP presented in this paper supports a wide range of different air-interface operations for different air-interfaces like OFDM/A or SDMA and is not tailored to a specific standard but to wireless communication standards in general. For performance evaluation, the A-FEP is compared to three different solutions which are

- the **C-FEP** which is a programmable DSP version of the FEP and the ancestor of the A-FEP. The comparison of C-FEP and A-FEP illustrates the performance gain obtained on the ExpressMIMO platform when using the latter instead.
- the IEEE 802.11a/n ASIP solution for single and multiple antennas implemented at ETH Zürich and presented in [7] is a well known ASIP architecture of high performance. It is further denoted as **ASPE A**.
- the recently published ASIP solution developed by the Cairo University [6] used for synchronization and acquisition in OFDM receiver systems which is called **Sync-ASIP**.

3.1. C-FEP

A first architecture of the C-FEP has already been presented in [15]. Since then, its design has been continuously improved to get a higher performance and a higher runtime flexibility. Like the A-FEP, the C-FEP is embedded in the standardized DSP shell but instead of using a Program Memory, the DSP engine is programmed through the control registers being part of the CSS. Other differences are listed in the following:

- **Processing Unit:** Besides the vector processing unit the C-FEP additionally embeds a DFT / IDFT unit and supports a component-wise look up table operation to approximate non-linear operations like invert or sine. The processing core is split over two identical processing units, each embedding twenty-four 25 x 18 bit signed multipliers and twelve 43 bit accumulators, which can either be used to implement two radix-4 butterflies for DFT / IDFT computation or to execute the different vector operations. The resulting pipeline consists of 15 stages and has to be emptied before the next vector operation can be executed. This results in an overhead of 11 to 16 cycles needed for initialization and termination of each vector operation.
- **MSS:** For DFT / IDFT support, the MSS is extended by twiddle factor and temporary data memories with an overall size of 52 kB.

On large vectors the ratio between the communication overhead and the processing time is close to zero while it results in a significant performance drop when processing standards operating on short data sets. Overcoming this drawback was the main motivation in designing the A-FEP solution being presented in the context of this paper.
The current target architecture of the baseband processing engine is a Xilinx Virtex 5 LX330 FPGA with a speed grade of -2. Although, an ASIC target technology may be considered for a future release[2]. For the FPGA target, processing engine and MSS of the C-FEP have been synthesized with Precision RTL from Mentor Graphics. The design obtains a frequency of 96 MHz by requiring 20119 function generators, 5030 CLB slices, 10945 DFFs, 33 block RAMs and 24 DSP48E slices.
For the ASIC target, only the processing engine of the C-FEP has been synthesized as the new design of the MSS is still part of our ongoing work. The maximum achievable frequency in this case is about 450 MHz and the area is 0.48 mm^2.

3.2. ASPE A

The ASIP solutions presented in [7] are based on the Adaptive Stream Processing Engine (ASPE) [16] which is a coarse-grained ASIP architecture being optimized for data processing. Main advantages are the shortened design time and the limited runtime reconfigurability for bug fixes resulting in lower costs than other solutions. The ASPE is connected to a GPP taking care of the control and of performance uncritical tasks. In contrast to the ExpressMIMO platform, ASPE designs include three different types of building blocks whose quantity and type can be selected from a library at design time.

1. **Functional Units** (FU) contain the arithmetic operations and can be combined to implement more complex ones. The number of internal pipeline stages is flexible and can be chosen at design time.

[2] 65nm target library, low power and high voltage threshold, characterized for a typical manufacturing process at 1.2 Volts power supply and 25°C temperature

2. **Storage Units** (SU) are used for local data storage. They are connected to the FUs via a runtime configurable network.

3. **Sequencer Units** (SEQ) control the configurable network between FUs and SUs. They further support control related tasks like zero-overhead loops or data dependent control flow.

In [7], two different ASIP solutions are presented that are both tailored to the processing of the IEEE 802.11a/n standard. The first one is a Single Input Single Output (SISO) receiver while the second one supports a 2x2 MIMO (Multiple Input Multiple Output) configuration. Table 1 illustrates the common ASPE configuration (ASPE A) for both designs. By combining the different FUs, the functionality of the ASPE A has been enhanced by a set of different vector operations like CORDIC for instance.
For a 0.13 μm CMOS target process, the SISO receiver configuration obtains a frequency of 160 MHz and requires a silicon-area of 1.9 mm^2. Instead the MIMO receiver has been synthesized for a 0.18 μm CMOS target process. For a target frequency of 160 MHz the silicon area is 7.6 mm^2, while the maximum achievable frequency is 250 MHz.

3.3. Sync-ASIP

The ASIP solution presented in [6] covers synchronization and acquisition of different OFDM standards. The design includes six 12 bit real adders, three 13 bit real multipliers, two 12 bit rounder, two 24 bit accumulators, ten 13 bit multiplexers and two 24 bit shifters that are distributed over three different pipeline stages. The maximum vector length supported is 256. Like ASPE A, the Sync-ASIP allows the processing of the CORDIC algorithm as well as maximum likelihood or correlation functions. The MSS is built of 286 word dual-port banks à 24 bit which is based on the choice of the maximum correlation length of 256 which is required for IEEE 802.16e and LTE. The instruction-set is composed of program flow instructions, optimized instructions to facilitate the implementation of the synchronization tasks and vector instructions.
For a 0.18 μm CMOS target process, the obtained frequency is 120 MHz and the area is 1.1 mm^2.

4. A-FEP ARCHITECTURE

4.1. Processing Engine Requirements

The front-end processing requirements for the support of OFDM/A, SC-FDMA, W-CDMA and SDMA have already been detailed in [1] and [15]. These papers state that the operations to be performed by the FEP on the transceiver side comprise among others channel estimation and synchronization which can be build up from component-wise vector operations and a DFT / IDFT unit. The latter is neglected for the A-FEP and kept as a separate processing engine in the baseband design of the ExpressMIMO platform.

Table 1. ASPE A Configuration

Ressource	Quantity	Comments
SEQ	1	program memory to store - the program control flow - the 16 bit command words
FU	1	complex-valued multiply and accumulate unit
	2	complex-valued arithmetic logic units
SU	1	registerfile (16 registers)
	1	input data buffer (64x32 bit)
	6	data storage (256x32 bit)

Table 2. A-FEP Vector Operations

Component-Wise Addition	$Z[i] = X[i] + Y[i]$
Component-Wise Product	$Z[i] = X[i] \times Y[i]$
Component-Wise Square Absolute	$Z[i] = \|X[i]\|^2$
Move	$Z[i] = X[i]$
Component-Wise Division	$Z[i] = X[i]/Y[i]$
Vector Sum	$Z = \sum X[i]$

The basic set of vector operations to be supported by the A-FEP is listed in Table 2. Besides, shift, max/min and argmax/argmin operations are provided that can operate independently on the real and imaginary parts of the vector elements being processed. In addition, pre- and post-processing value modifications are applied, comprising absolute value, negation, zeroing, rescaling and saturations. The input and output vector elements can be of four different data types: 8 or 16 bit signed integers and complex numbers with a size of 16 or 32 bit. Type conversions between them are specified through parameters being part of the instruction word.
One major challenge when supporting a wide range of different standards is to ensure that all of them meet their real-time constraints. Therefore, the A-FEP comes with a programmable Address Generation Unit (AGU) that allows to build input vectors from non-contiguous data sets in the connected MSS. Symmetrically, the AGU can also be used to store result vectors at non-contiguous locations, allowing component skipping or (periodic) value repetition. Moreover, programmable self-wrapping mechanisms allow to turn MSS sections into circular buffers. Major parts of the MSS are the 4 kB program memory and the input-output data space which has been designed for the support of standards which operate on large vector sizes like LTE or DAB. It is split over four different memory banks, each with a size of 4096 32 bit entries. The maximum vector length that can be processed depends on the data type. For vector elements with a size of 32 bit the maximum length is 4096 while it is 16384 for a size of 8 bit.

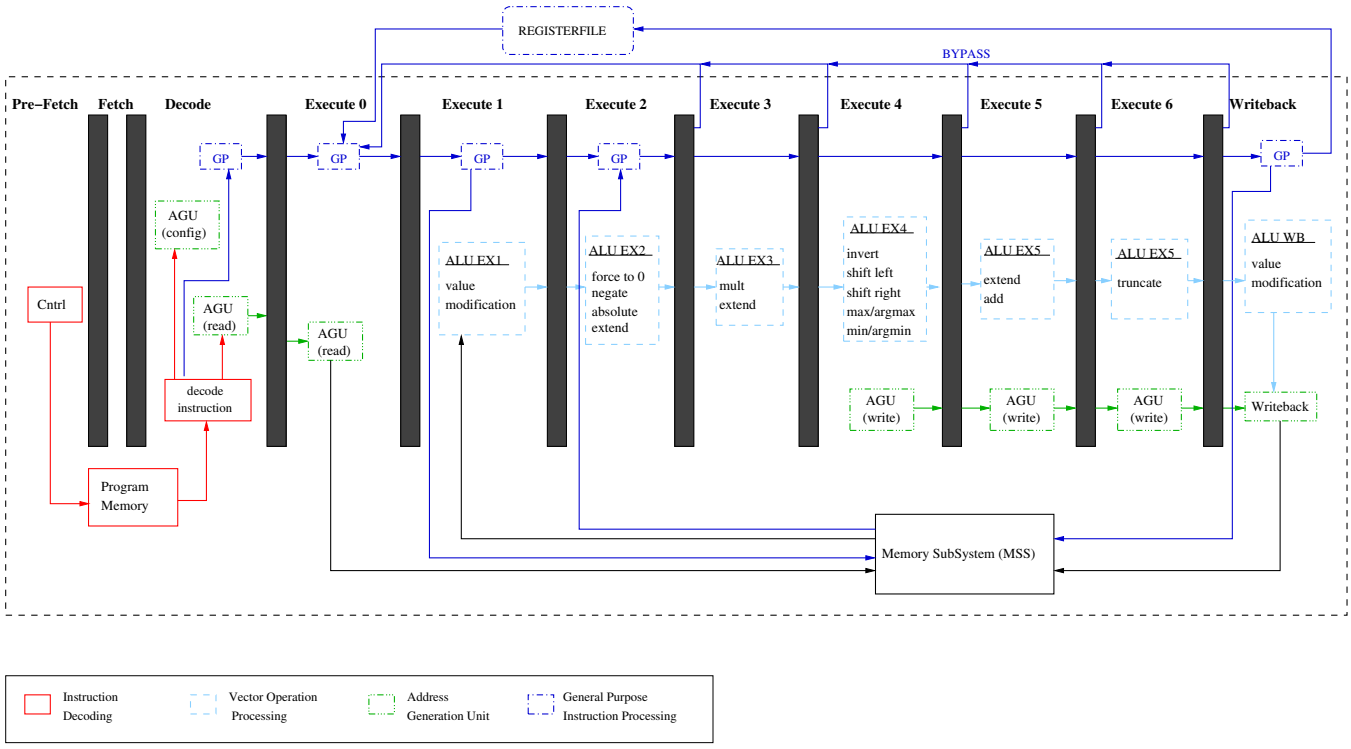

Fig. 3. A-FEP Pipeline

4.2. HW Architecture and Instruction-Set

The instruction-set of the A-FEP comprises three different instruction types:

1. **AGU configuration instructions:** These instructions carry the necessary parameters for programming the AGU. Six different instructions have been implemented whose quantity in the program code may vary depending on the amount of parameters to be modified for the subsequent arithmetic vector processing instruction.

2. **Arithmetic Vector Processing (AVO) instructions:** To fulfill the processing engine requirements, the A-FEP supports nine different AVO instructions which are vector multiplication, addition, square, square modulus, sum, shift, move, division and max,min. Maximum supported vector length is 16384 entries for a vector composed of 8 bit vector elements.

3. **General Purpose (GP) instructions:** The GP instruction-set is based on a load-store architecture and supports common instructions like compare, branch or ALU operations. It comes with a registerfile possessing a size of 16 x 32 bit. Further included is an IRQ instruction used to signal the main CPU the end of a scheduled task. Tasks can represent a single instruction or more complex algorithms like packet synchronization. Letting the main control to the main CPU comes with the advantage of a simplified scheduling when processing different standards in a multimodal fashion.

The pipeline structure is illustrated in Fig. 3. It consists of eleven stages and comes with a throughput of two vector elements per cycle. Usually, one instruction per cycle is fetched from the program memory. An exception are the multicycle AVO instructions which may operate on vectors with variable length. While executing these instructions, the pipeline registers between *Pre-Fetch*, *Fetch* and *Decode* are stalled.
Synthesizing the A-FEP for the FPGA target, it obtains a frequency of 105 MHz by requiring 13122 function generators, 3281 CLB slices, 6433 DFFs, 17 block RAMs and 8 DSP48E slices. For the ASIC target, only the processing engine has been synthesized as the new design of the MSS is part of our ongoing work. The maximum achievable frequency is about 550 MHz, the area is 0.18 mm^2.

5. RUN-TIME PERFORMANCE COMPARISON

The runtime performance depends on two different factors: the processing time required for the communication between the main CPU and the baseband DSP engines and the pure data processing time of the DSPs. For a standard operating on small vector lengths (e.g. IEEE 802.11a/p), the first factor is of major importance while it is more or less negligible

for standards like LTE that operate on large vectors. Table 3 lists the A-FEP execution times for different front-end processing algorithms of a IEEE 802.11p receiver for a frequency of 100 MHz. Packet structure and the applied OFDM decoding procedure have recently been presented in [17].

Table 3. A-FEP Execution Times (802.11p Receiver)

algorithm	cycles	execution time
energy detection	302	3.06 μs
channel estimation	45	0.45 μs
data detection (16-QAM, init)	172	1.72 μs
data detection (16-QAM)	114	1.14 μs
data detection (64-QAM, init)	219	2.19 μs
data detection (64-QAM)	342	3.42 μs

For demonstration and to compare the performance of the different presented solutions we will further take the example of two different packet detection algorithms for OFDM signals.

5.1. Auto-correlation Based Packet Detection (A-PD)

In [7], packet detection is performed over the Short Training Sequence (STS) of the IEEE 802.11a/n packet illustrated in Fig. 4. The STS is composed of ten repetitions of a 16 samples sequence. The applied algorithm correlates L samples of the received sample stream $r[d]$ (d is the time index) with the subsequent L ones. For a single antenna receiver this can be expressed via the auto-correlation function

$$P_L[d] = \sum_{m=0}^{L-1} (r^*[d+m] \cdot r[d+m+L]) \tag{1}$$

To obtain a high accuracy, L is set to half of the size of the STS which corresponds to a vector length of 80 samples. Next, the average energy of the received sample stream in the actual window is calculated as

$$R_L[d] = \sum_{m=0}^{L-1} |r[d+m+L]|^2 \tag{2}$$

In case

$$|P_L[d]|^2 > \frac{|R_L[d]|^2}{2} \tag{3}$$

the beginning of the packet is found. Otherwise the window over the incoming sample stream is shifted by a predetermined number of samples. Extending this algorithm to the 2x2 MIMO case, (1) and (2) are performed for both receive chains. The comparison is performed over the average results stated as

$$P_{L,\text{avg}}[d] = \frac{1}{2} \sum_{j=1}^{2} P_{jL}[d] \tag{4}$$

and

$$R_{L,\text{avg}}[d] = \frac{1}{2} \sum_{j=1}^{2} R_{jL}[d] \tag{5}$$

For the A-FEP, the set of instructions to be executed and the cycle counts for each of them for the SISO case are shown in Table 4. The total amount of cycles are $6 \cdot \frac{L}{2} + 72$ when including the GP instructions and $6 \cdot \frac{L}{2} + 24$ if only the data processing is taken into account. When using the C-FEP instead the implementation can be simplified as illustrated in Table 5. Considering only the pure data processing without the communication overhead, the resulting amount of cycles in this case is $4 \cdot \frac{L}{2} + 46$.

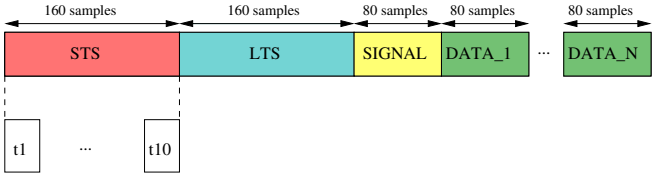

Fig. 4. IEEE 802.11a Packet Structure

Table 4. A-FEP Instructions (A-PD)

	instructions	cycles
$P_L[d]$	agu_cfg (6x)	9
	vec_move	L/2 + 4
	agu_cfg (4x)	4
	vec_mult	L/2 + 4
	agu_cfg (2x)	2
	vec_sum	L/2 + 4
$R_L[d]$	agu_cfg (2x)	2
	vec_square_modulus	L/2 + 4
	agu_cfg (2x)	2
	vec_sum	L/2 + 4
	agu_cfg (2x)	2
	vec_square_modulus	L/2 + 4
$\|P_L[d]\|^2 > \frac{\|R_L[d]\|^2}{2}$	nop (7x)	7
	lw	5
	nop	1
	lw	5
	nop	1
	bgt	8

Table 5. C-FEP Operations (A-PD)

	operations	cycles
$P_L[d]$	move	L/2 + 11
	multiplication + sum	L/2 + 12
$R_L[d]$	square_modulus + sum	L/2 + 12
$\|P_L[d]\|^2 > \frac{\|R_L[d]\|^2}{2}$	square_modulus + sum	L/2 + 11

Table 6. Design Comparison (A-PD)

Solution	cycles (SISO)	cycles (MIMO)	execution time (SISO)	comm. overhead (SISO)	execution time (MIMO)	comm. overhead (MIMO)
ASPE A	296	650	2.96 μs	-	6.5 μs	-
A-FEP	264	572	2.64 μs	0.48 μs	5.72 μs	0.64 μs
C-FEP	312	465	3.12 μs	1.2 μs	4.65 μs	1.2 μs

To get an idea about the time required for the communication overhead, different measurements have been carried out on the ExpressMIMO platform for a frequency of 100 MHz.

- The time required by the main CPU to program one vector operation of the C-FEP takes 420 ns. The communication overhead can be reduced when programming the subsequent vector processing operation during the execution of the previous one.
- Using polling, the time till the main CPU reacts on the end of a C-FEP vector operation is 436 ns.
- The time necessary to copy two values to the main CPU and to compare them is 350 ns.

To sum up, Table 6 gives the resulting cycles counts and processing times for a frequency of 100 MHz. Based on these results it can be observed that for this algorithm, the A-FEP performs slightly better than ASPE A although the architecture of the latter is optimized for the processing of the IEEE 802.11a/n standard. Compared to the C-FEP, the A-FEP reduces the communication overhead significantly due to reduced pipeline delays and due to the GP instructions. The development of algorithmic implementations is thus simplified using the A-FEP as no explicit synchronization between the processing unit and the main CPU is needed. Considering only the data processing time, the C-FEP performs better as the sum is not an extra operation.

5.2. Energy Based Packet Detection (E-PD)

In the first example, we compared the A-FEP to two powerful ASPE A solutions that are able to execute the whole baseband processing of the applied standard. Now, the A-FEP is compared to a specialized ASIP for synchronization and acquisition that has recently been published in [6]. The applied packet detection algorithm is slightly different than the previously presented one. To get a first estimate of the probability that the beginning of the packet is detected, two energy values a and b are calculated over $L = 64$ elements and divided through each other. In case the result is beyond a certain threshold, the exact beginning of the packet is detected using auto-correlation functions. The energy values can be computed as

$$a = \sum_{n=0}^{L-1} |r_{n-L}|^2 \tag{6}$$

and

$$b = \sum_{n=0}^{L-1} |r_{n+L}|^2 \tag{7}$$

while their relation is expressed as

$$m = \frac{a}{b} \tag{8}$$

For the A-FEP, the set of instructions to be executed is illustrated in Table 7. Including the GP instructions, the total amount of cycles is $3 \cdot \frac{L}{2} + 68$ and $3 \cdot \frac{L}{2} + 12$ if only the data processing is taken into account. When using the C-FEP instead the implementation can be simplified as illustrated in Table 8 and the processing times for a frequency of 100 MHz are provided in Table 9. As expected, the typical phenomenon can be observed that a weakly programmable ASIP specialized for a specific task performs far better than a flexible ASIP solution that is capable to perform a wide range of different operations. Comparing the A-FEP with the C-FEP solution it can be seen, that the A-FEP drastically reduces the communication overhead for short data sets.

Table 7. A-FEP Instructions (E-PD)

	instructions	cycles
a,b	agu_cfg (6x)	9
	vec_abs_square	L/2 + 4
	agu_cfg (2x)	2
	vec_abs_square	L/2 + 4
	agu_cfg (2x)	2
	vec_sum	L/2 + 4
m	agu_cfg (4x)	2
	vec_cwl	7
	agu_cfg (3x)	3
	vec_mult	4
	nop (7x)	7
	lw	5
	nop	1
	lw	5
	nop	1
	bgt	8

Table 8. C-FEP Operations (E-PD)

	instructions	cycles
a,b	vec_abs_square + sum	L/2 + 12
	vec_abs_square + sum	L/2 + 12
m	vec_cwl	15
	vec_mult	11

Table 9. Design Comparison (E-PD)

Solution	cycles	execution time	communication overhead
Sync-ASIP	31	0.31 μs	-
A-FEP	108	1.08 μs	0.56 μs
C-FEP	114	1.14 μs	2.29 μs

6. CONCLUSION

In this paper we focused on the comparison of two new designs for the Front-End Processor for the OpenAirInterface ExpressMIMO platform with existing ASIP solutions. Comparing the A-FEP to the C-FEP, we have shown that the A-FEP performs better in terms of processing time due to the reduced communication overhead with the host system and due to reduced internal latencies. Although the A-FEP supports a wide range of different wireless communication standards, we have shown that it performs slightly better for a packet detection algorithm than a solution presented by ETH Zürich that is tailored to the processing of the IEEE 802.11a/n standard. On the other hand the performance is still worse when compared to an ASIP solution designed for synchronization and acquisition that comes with a reduced instruction-set and is therefore less flexible than the presented A-FEP. Future work includes the design analysis with regards to energy consumption and power dissipation as well as the final integration of the A-FEP on the ExpressMIMO platform.

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