Chip-Sparsification and Symbol-Equalization for WCDMA Downlink

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***Abstract*—We consider SINR maximizing receivers based on the concept of chip-level filtering and symbol level equalization for WCDMA downlink. In this contribution we propose a new class of receivers based on *channel sparsifying* linear pre-processing at chip-rate followed by time-varying symbol level equalizers. Due to a sparse structure imposed on the channel (i.e. *sparsification*) by a chip level pre-equalizer filter which we call *channel sparsifier*, the effective channel after despreading presents itself as a symbol-level ISI channel. Time-varying equalization at symbol level is necessitated by the presence of aperiodic scrambler which is treated as deterministic. The optimal channel sparsifier maximizes SINR at the output of symbol level equalizer. We focus here on downlink channels that have significant dispersion in the temporal domain. Expressions for post processing SINRs (after channel sparsification, despreading and subsequent symbol level equalization) are derived for all receivers and used for performance evaluation. We show that improved receivers for WCDMA downlink can be designed benefiting from a combination of generalized channel sparsification, deterministic treatment of scrambler and non-linear equalization.**

I. Introduction

Optimal linear receivers for WCDMA are symbol level (deterministic) time-varying multiuser receivers that are known to be prohibitively complex. One class of such receivers is based on symbol-level multiuser detection (MUD) where linear or non-linear transformations can be applied to the output of a channel matched filter (RAKE). Linear methods in this category are decorrelating and MMSE MUD both known to deal with inverses of large time-varying code cross-correlation matrices across symbols and thus are impractical. Non-linear MUD methods focus on estimating, reconstructing and subtracting signals of interfering codes. They are in general called interference canceling (IC) methods and known sub-categories among them are serial and parallel interference cancelers (SIC/PIC) (see [1] for MUD).

A less complex alternative is *dimensionality reducing* linear chip equalization followed by further nonlinear interference canceling or joint detection stages to improve symbol estimates [2] (and references therein). The basis for these receivers is that interference arises from loss of orthogonality due to the multipath channel and this problem is effectively solved by attempting to bring back the orthogonality through a *SINR-maximizing* LMMSE equalizer (or a MMSE-ZF solution). Gains obtained by this two-step design over classical chip-equalization are limited by the efficacy of the dimensionality reduction achieved at the output of linear chip equalizer and also by the type of processing at symbol level.

A solution of the second category can intuitively be treated as a dimensionality-reduction stage in MUD. It may take the form of a general chip-level filter carrying out functions of channel equalization or indeed a spatio-temporal $\rightarrow$ spatial channel-shortener (e.g., $2N \times 2$ to 2×2 in MIMO HSDPA) [3]. This stage precedes either per-code joint detection of data streams at symbol level [4] [3] or can be followed-up by one of the several possible decision-feedback approaches [5]. In the general MIMO case, the resulting symbol-rate spatial channel can now be seen as only a per-code spatial mixture to which simplified (per-code) processing can be applied. Assuming L to be the processing gain, N_t the number of TX streams, N_r the number of RX antennas, and p to be the oversampling factor *w.r.t.* the chip rate, this can be seen as a dimensionality-reduction from $p \cdot L \cdot N_r$ to N_t. Given this drastic reduction, it is not surprising to see performance falling well short of optimal time-varying symbol-level processing (linear and non-linear MUD solutions). Despite their performance shortcomings, one may nevertheless point out that complexity/performance tradeoff between MUD and chip-level type receivers favors the latter, which for this reason are well-accepted in practical receiver designs [3]. In general, dimensionality reduction can range from $p \cdot L \cdot N_r$ to N_t, to $K \cdot N_t$ or to $K \cdot N_f \cdot N_t$, where K is the number of codes per stream, and N_f is an arbitrary number of symbols of the any code stream. Subsequent non-linear processing again depends upon the achievable performance/complexity tradeoff desired.

In this paper we take the approach of optimally combining chip-level and symbol-level processing and investigate receivers based on channel sparsification as opposed to channel shortening. The chip-level channel is conditioned using a pre-equalizer in order to tradeoff achievable gains at the symbol level equalizer with the associated complexity. The idea itself is not new and dates as far back as early 70's [6] [7] [8] where combined equalization and maximum-likelihood sequence estimation (MLSE) was considered in order to achieve higher data-rates. More recently, Al-Dhahir et.al [9] proposed a unified approach for design of finite length *channel shortening* MMSE equalizers as pre-filters for reduced-order MLSE. In all these contributions, the design goal was to find optimal pre-equalizers that *shorten* the channel impulse response (CIR) to

a desired target impulse response (TIR) of specified length. The pre-filters are based on different optimization and design constraints. For instance [6] minimizes the error variance at the output of the pre-filter subject to energy constraints on the TIR, [7] attempts the same while imposing a monocity constraint on the TIR and [8] proposes to render the error white so as to obtain optimal performance for the ML stage. On the other hand, in this paper, we do not interest ourselves in shortening the CIR, instead we impose a structured sparsity criterion on the resultant sparse impulse response (SIR). This paper focuses on a class of HSDPA receivers based on *channel sparsifying* linear pre-processing, and introduces a time-varying model of the resulting reduced-dimensional (symbol-rate) temporal channel. The sparsification is controlled by an appropriate design criterion for the chip-level channel sparsifier and time-variant model is a consequence of treating the scrambler as deterministic [10]. The cascade, as for the case of classical chip-equalizer front-end, results in a reduced-parameter problem the dimensionality of which can be controlled through sparsifier design. While the classical MMSE chip-equalizer is highly effective in mitigating the effects of temporal dispersion of the channel and restoring orthogonality of codes, it works on the principle of optimally combining the channel power in a single tap corresponding to the target equalizer delay thereby excluding the possibility of any "Viterbi-like" post processing at later stages. In this contribution we show that improved receivers for WCDMA downlink can be designed benefiting from a combination of generalized (and controlled) channel sparsification, deterministic treatment of scrambler and reduced-parameter non-linear detection.

II. Downlink Signal Model

Fig. 1 illustrates the equivalent baseband chip-level downlink signal model. The received signal vector (chip-rate) at the

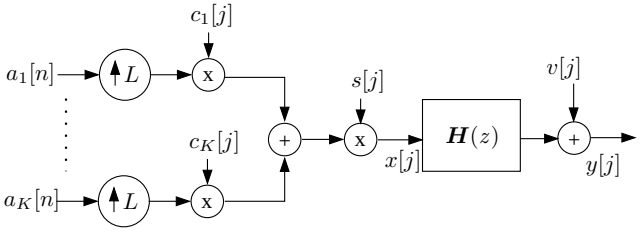

Fig. 1. Downlink signal model.

UE can be modeled as

$$y[j] = \boldsymbol{H}(z)x[j] + v[j], \tag{1}$$

In this model, j is the chip index, $\boldsymbol{H}(z)$ is the frequency selective channel, the output of which, is sampled p times per chip and $v[j]$ represents the vector of noise samples that are zero-mean circular Gaussian random variables. The sequence $x[j]$ introduced into the channel is expressed as

$$x[j] = \sum_{k=1}^{K} s[j]c_k[j \mod L]a_k[n] \tag{2}$$

where k is the code index, n is the index of the symbol on code k given by $n = \lfloor \frac{j}{L} \rfloor$, L is the spreading factor (we consider $L = 16$ as in HSDPA), c_k is a unit-norm spreading code, and $s[j]$ the scrambling sequence element at chip time j, which is zero-mean *i.i.d.* with elements from $\frac{1}{\sqrt{2}}\{\pm 1 \pm j\}$. Consider estimation of the symbol sequence, $a_k[n]$, of the k^{th} code among K codes in a SISO/SIMO channel. Fig. 2, represents a simple vectorized TX signal model where $\boldsymbol{x}[n]$ is the chip vector defined as $\boldsymbol{x}[n] = [x_0[n] \cdots x_{L-1}[n]]^T$, where $x_i[n]$ is the i^{th} multi-code (K codes) chip corresponding to the n^{th} symbol, $a[n]$. If the delay spread is N chips, and

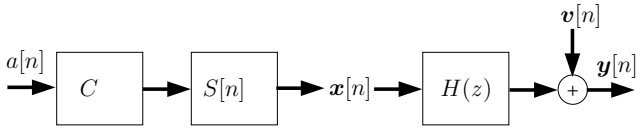

Fig. 2. Simplified TX signal model.

the sparsifier length in chips is E, assuming an oversampling factor of p, the block-Toeplitz (FIR) channel $\mathcal{T}(\boldsymbol{H})$ is a $pE \times N + E - 1$ block Toeplitz channel convolution matrix. The channel-sparsifier cascade results in a equivalent sparse impulse response that we denote by $\boldsymbol{g}$. By design, $\boldsymbol{g}$ has dominant tap gains at chip offsets $d + \nu L$ where $\nu \in \{0, 1, \ldots N_f - 1\}$. and arbitrary non-zero values in all other taps. We can now define $\boldsymbol{G}_\nu$ the $L \times L$ Toeplitz matrix with $[g[d+\nu L], g[d+\nu L+1], \ldots, g[d+(\nu+1)L-1]$ as the first row and $[g[d+\nu L], g[d+\nu L-1], \ldots, g[d+(\nu-1)L+1]^T$ as the first column and matrices $\boldsymbol{G}_{\nu,s}$ and $\overline{\boldsymbol{G}}_\nu$ given by

$$\boldsymbol{G}_{\nu,s} = \boldsymbol{G}_\nu - \overline{\boldsymbol{G}}_\nu \tag{3}$$

where $\boldsymbol{G}_{\nu,s}$ is a diagonal matrix with $g[d + \nu L]$ on the diagonal and $\overline{\boldsymbol{G}}_\nu$ is $\boldsymbol{G}_\nu$ with the diagonal set to zero. As shown in Fig. 3, the channel sparsifier output serves as input to the descrambler-correlator bank (after an appropriate delay not depicted in the figure in the interest of simplicity). The

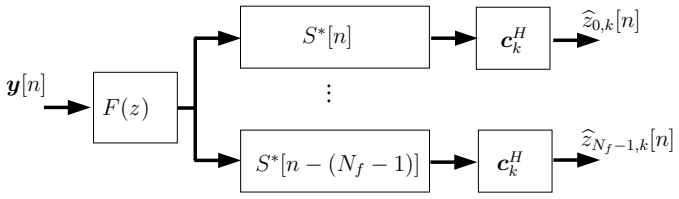

Fig. 3. SISO RX model.

dependence of the output $\widehat{z}_{m,k}[n]$, $m \in \{0, 1, \ldots N_f - 1\}$ of each descrambler-correlator pair in the bank on the scrambler vector at n results in a time-varying symbol level channel. The expression for $\widehat{z}_{m,k}[n]$ can be derived as in (4) where we denote by $g[\nu]$ the tap-values of $\boldsymbol{g}$ at $d + \nu L$.

III. Generalized Channel Sparsification

As discussed earlier, the chip-level sparsifier conditions the channel to have an approximately sparse structure. We say it is approximately sparse because the resultant channel has N_f

dominant taps and all other taps have arbitrary small non-zero tap gains. While we do not constrain the position of first dominant tap, we do constrain the remaining taps to be regularly spaced L chips apart where L denotes the downlink spread factor. Furthermore, the channel sparsifier should be a solution to an appropriately chosen optimization criterion which in our case is the post-processing SINR. The channel sparsifying filter is thus chosen so as to maximize the SINR at the output of symbol-level equalizer. The optimum chip-level channel sparsifying filter is therefore a function of symbol level equalizer.

Before we go further, we define by $\widetilde{\boldsymbol{H}}$, the matrix whose columns are formed by the L-spaced N_f columns of $\mathcal{T}(\boldsymbol{H})$ and are the columns of the channel convolution matrix at precisely the chip-position offsets at which the resultant sparse impulse response will have dominant taps. We define the matrix $\overline{\mathcal{T}}(\boldsymbol{H})$ as the matrix formed by setting these columns to zero in $\mathcal{T}(\boldsymbol{H})$. For the specific case of $N_f = 2$, $\overline{\mathcal{T}}(\boldsymbol{H})$ has 2 columns at equalizer/sparsifier delay d and $d + L$ that we shall denote henceforth by $\boldsymbol{h}_0$ and $\boldsymbol{h}_1$. We also define the positive definite matrix $\boldsymbol{B}$ as

$$\boldsymbol{B} = \sigma_{tot}^2 \overline{\mathcal{T}}(\boldsymbol{H})\overline{\mathcal{T}}(\boldsymbol{H})^H + \boldsymbol{R}_{vv}. \tag{5}$$

These two matrices are of special significance to us. We shall see later that these matrices are the common link to all the different channel-sparsifier/symbol-equalizer pairs. In fact, the channel sparsifier for all three receivers lives in the column span of the product matrix $\boldsymbol{B}^{-1}\widetilde{\boldsymbol{H}}$. A fact that we shall exploit in computing the optimum channel sparsifier.

The philosophy behind the proposed receiver structures can be summed up as follows. The channel is rendered sparse by chip-level processing so that this chip-level sparse channel can be exploited by reduced complexity non-linear equalization that operates at symbol level. It is the presence of the aperiodic scrambler that adds to the complexity of the receiver. This type of combined chip and symbol level equalization can provide gains only if the scrambler is treated as deterministic, otherwise, the random scrambler assumption will compel us to treat the time varying signal contribution as noise. For a specific symbol-level equalizer, the post-processing SINR is derived. In the sequel, we will see that this leads to an optimization problem with a quadratic constraint and a quadratic cost function and takes the general form

$$\max_{\boldsymbol{f}} \frac{\boldsymbol{f}^H \boldsymbol{A} \boldsymbol{f}}{\boldsymbol{f}^H \boldsymbol{R} \boldsymbol{f}} \text{ subject to } \boldsymbol{f}^H \boldsymbol{A} \boldsymbol{f} = \text{constant}, \tag{6}$$

The solution to this maximization problem is well known to be the maximum generalized eigenvector of the matrix pair $(\boldsymbol{A}, \boldsymbol{R})$.

IV. SISO HSDPA Receiver Structures

A. Receiver 1: MMSE Chip Equalizer-Correlator

As is well known, LMMSE equalizer is the optimal linear equalizer that attempts to suppress all Inter-Chip Interference (ICI). The linear FIR MMSE chip-level equalizer tries to obtain chip estimates and is given by the standard expression $\boldsymbol{f} = \boldsymbol{R}_{\boldsymbol{xy}}\boldsymbol{R}_{\boldsymbol{yy}}^{-1}$ (see fig. IV-A). We can write the equalizer output as the sum of an arbitrarily scaled desired term and an error term

$$\widehat{x}[j] = x[j] - \widetilde{x}[j], \tag{7}$$

The error $\widetilde{x}[j]$ is a zero-mean complex normal random variable.

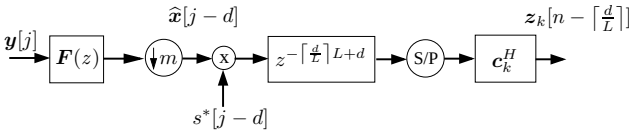

Fig. 4. LMMSE equalizer and correlator.

As shown in Fig. IV-A, at the output of the equalizer, the estimate of the chip sequence in (7), is obtained after a delay d equal to the equalization delay in chips. After despreading (for the k^{th} code) the signal at the symbol level is written as

$$z_k[n] = a_k[n] - \widetilde{z}_k[n] = g[0]a_k[n] - \widetilde{z}_k[n], \tag{8}$$

$g[0]$ in this expression is defined as in section II

The SINR at output of the LMMSE chip equalizer/correlator is thus given by

$$SINR = \frac{\sigma_k^2 |g[0]|^2}{\sigma_{tot}^2 \|\overline{\boldsymbol{g}}\|^2 + \sigma_v^2 \boldsymbol{f}^H \boldsymbol{f}}, \tag{9}$$

where $\overline{\boldsymbol{g}}$ is computed by setting $g[0]$ in $\boldsymbol{g}$ to 0 and $\sigma_{tot}^2 = \frac{1}{L}\sum_{k=1}^{K} \sigma_k^2$.

B. Receiver 2: PIC + ML equalization post sparsification

For the rest of the receiver structures we consider deterministic treatment of the scrambler. In section III we introduced channel sparsification that will remain the common pre-processing stage for all the following receiver structures though the criteria for channel sparsifier design might differ.

At each of the descrambler-correlator pairs, $N_f - 1$ dominant taps are not aligned to the de-scrambler in question and hence experience inter-code interference. For ML equalization of the N_f-tap sparsified channel for the code of interest k, the inter-code interference (MUI) present on $N_f - 1$ mis-aligned taps can be canceled by an iterative MUI cancellation algorithm

$$\begin{aligned}\widehat{z}_{m,k}[n] = g[m]a_k[n-m] + \sum_{\nu \neq m} g[\nu]\boldsymbol{c}_k^H S_n^H S_{n-\nu}\boldsymbol{c}_k a_k[n-\nu] + \sum_{j \neq k}\sum_{\nu \neq m} g[\nu]\boldsymbol{c}_k^H S_n^H S_{n-\nu}\boldsymbol{c}_j a_j[n-\nu] + \\ \sum_{j \in K} \boldsymbol{c}_k^H S_n^H \overline{\boldsymbol{G}}_m S_n \boldsymbol{c}_j a_k[n-m] + \sum_{j \in K}\sum_{\nu \neq m} \boldsymbol{c}_k^H S_n^H \overline{\boldsymbol{G}}_\nu S_{n-\nu}\boldsymbol{c}_j a_j[n-\nu] + \boldsymbol{f}^H \boldsymbol{v}[n],\end{aligned} \tag{4}$$

say, PIC. With such a processing stage preceding ML equalization, the ML processing will now be strictly on a per-code basis. Furthermore, we make the following assumptions at the output of the deterministic de-scrambler; the signal and interference terms are uncorrelated, the interference plus noise components are uncorrelated across $\widehat{z}_{0,k}[n]$ and $\widehat{z}_{1,k}[n]$, $g[1]\boldsymbol{c}_k^H S_n^H S_{n-1} c_k a_k[n-1]$ and $g[0]\boldsymbol{c}_k^H S_{n-1}^H S_n c_k a_k[n]$ are independent for all pairs of n and $n-1$ and the interference plus noise components are themselves uncorrelated across symbol durations. If we then define a matrix $\boldsymbol{A}$ as

$$\boldsymbol{A} = \sigma_k^2 \left(1 + \frac{1}{L}\right) \widetilde{\boldsymbol{H}} \widetilde{\boldsymbol{H}}^H, \tag{10}$$

and $\boldsymbol{B}$ as in (5) the per-code $SINR$ is given by

$$SINR_k = \frac{\boldsymbol{f}^H \boldsymbol{A} \boldsymbol{f}}{\boldsymbol{f}^H \boldsymbol{B} \boldsymbol{f}}, \tag{11}$$

Clearly, the filter $\boldsymbol{f}$ that maximizes (11) is the eigenvector corresponding to the maximum generalized eigenvalue $\lambda_{max}(\boldsymbol{A}, \boldsymbol{B})$.

1) Discussion: Indeed, if the inverse of $\boldsymbol{B}$ exists, $\boldsymbol{f}$ is also an eigenvector of $\boldsymbol{B}^{-1}\boldsymbol{A}$. In general, due to the particular structure of $\boldsymbol{A}$, the filter $\boldsymbol{f}$ is of the form

$$\boldsymbol{f} = \alpha \boldsymbol{B}^{-1} \boldsymbol{h}_0 + \beta \boldsymbol{B}^{-1} \boldsymbol{h}_1, \tag{12}$$

That $\boldsymbol{f}$ should completely live in the space spanned by $\boldsymbol{h}_0$ and $\boldsymbol{h}_1$ is not surprising, since it is obvious from the expression for per-code SINR that, any other $\boldsymbol{f}$ will increase then value of the denominator in (11) thus reducing the SINR.

C. Receiver 3: ML equalization post sparsification

Considering the computational complexity involved in an additional PIC stage in the receiver above, one is tempted to investigate the performance of ML equalization of the sparse channel without inter-code interference cancellation. Without the PIC pre-processing, however, the channel sparsifier design has to account for inter-code interference on the $N_f - 1$ misaligned taps in the descrambler-correlator bank. With same assumptions on correlation and independence of interference and noise terms as before, the $SINR_k$ for code of interest k for the case of $N_f = 2$ is given by (13)

$$SINR_k = \sigma_k^2 \sum_{i=0,1} \frac{\boldsymbol{f}^H \widetilde{H} \begin{bmatrix} \bar{i} + i/L & 0 \\ 0 & i + \bar{i}/L \end{bmatrix} \widetilde{H}^H \boldsymbol{f}}{\boldsymbol{f}^H \left\{ \boldsymbol{B} + \left(\sigma_{tot}^2 - \frac{\sigma_k^2}{L}\right) \boldsymbol{h}_{\bar{i}} \boldsymbol{h}_{\bar{i}}^H \right\} \boldsymbol{f}} \tag{13}$$

We choose $N_f = 2$ here with the sole intention of simplifying the SINR expression. The extension to $N_f > 2$ is trivial and straightforward. The optimum filter $\boldsymbol{f}$ that maximizes (13) in this case can be computed based on a 2-D search. Recall that the optimum filter lives in $span\{\boldsymbol{h}_0, \boldsymbol{h}_1\}$ and can be decomposed as (12). We also note that SINR is insensitive to any scale factor of $\boldsymbol{f}$, this allows us to set α (or for that matter β) to 1. The problem of finding the optimum filter thus reduces to finding the optimum β which can be a complex co-efficient and whose phase also influences the SINR. We therefore carry out a 2-D search for the optimum beta over an appropriate search grid and compute the optimum sparsifying filter using (12).

D. Receiver 4: Post sparsification MRC

We now draw attention to equation (4). Here too, *w.l.o.g*, we assume $N_f = 2$. Maintaining that code-k is our code of interest, we see that as a consequence of controlled ISI present in the sparse channel, scaled versions of the n^{th} symbol on code-k is present at $\widehat{z}_{0,k}$ at time n and at $\widehat{z}_{1,k}$ at time $n+1$. If we assume, as before, that inter-code interference has been canceled, and all other components of $\widehat{z}_{m,k}$ except the symbol of interest $a_k[n]$ as noise, the matrix $\boldsymbol{A}$ in the optimization problem is now given by

$$\boldsymbol{A} = \sigma_k^2 \widetilde{\boldsymbol{H}} \widetilde{\boldsymbol{H}}^H, \tag{14}$$

and $\boldsymbol{B}$ can be shown to be as in (15) and we arrive at the simplified SINR expression at the output of the maximum ratio combiner that is given by (16) below

$$\boldsymbol{B} = \sigma_{tot}^2 \sum_{i=0}^{1} \frac{|\boldsymbol{f}^H \boldsymbol{h}_i|^2}{|\boldsymbol{f}^H \boldsymbol{h}_0|^2 + |\boldsymbol{f}^H \boldsymbol{h}_1|^2} \overline{\mathcal{T}}_i(\boldsymbol{H}) \overline{\mathcal{T}}_i^H(\boldsymbol{H}) + \boldsymbol{R}_{vv} \tag{15}$$

$$SINR_k = \frac{\sigma_k^2 \left(\boldsymbol{f}^H \widetilde{\boldsymbol{H}} \widetilde{\boldsymbol{H}}^H \boldsymbol{f}\right)^2}{\sum_{i=0}^{1} |\boldsymbol{f}^H \boldsymbol{h}_i|^2 \boldsymbol{f}^H \left(\sigma_{tot}^2 \overline{\mathcal{T}}_i(\boldsymbol{H}) \overline{\mathcal{T}}_i^H(\boldsymbol{H}) + \boldsymbol{R}_{vv}\right) \boldsymbol{f}} \tag{16}$$

Where $\overline{\mathcal{T}}_i(\boldsymbol{H})$ is defined as the channel convolution matrix $\mathcal{T}(\boldsymbol{H})$ with the $d + iL$ column set to zero. Since the SINR is itself a function of channel sparsifier, the optimum channel sparsifying filter is computed in an iterative fashion. The iteration is initialized by using $\boldsymbol{f}$ that maximizes (11) to compute $\boldsymbol{B}$. The optimum filter $\boldsymbol{f}_{opt}$ is then computed by alternatively plugging in the maximum generalized eigenvector of the matrix pair $(\boldsymbol{A}, \boldsymbol{B})$ and recomputing the matrix $\boldsymbol{B}$ until convergence.

V. Simulation Results

We show here simulation results and compare the performance of the different receiver structures. In the first instance, for a fixed SNR and over several realizations of a frequency selective FIR channel $\boldsymbol{H}(z)$, we compute the SINRs at the output of the receivers and compare the distribution of SINRs for various receivers. The channel coefficients are complex valued zero-mean Gaussian of length 16 chips. The length of the channel sparsifying filter is the same as that of chip-equalizer. The per-user SINR is used as a performance measure for all receivers. In Fig. 5 we plot the SINR for receivers 1, 2 and 3. The SINR at the output of chip-equalizer correlator receiver is computed by treating the scrambler as random and compared with the distribution of SINR at the output of the other two receivers where the scrambler is treated as deterministic. In reality, deterministic treatment will imply that the

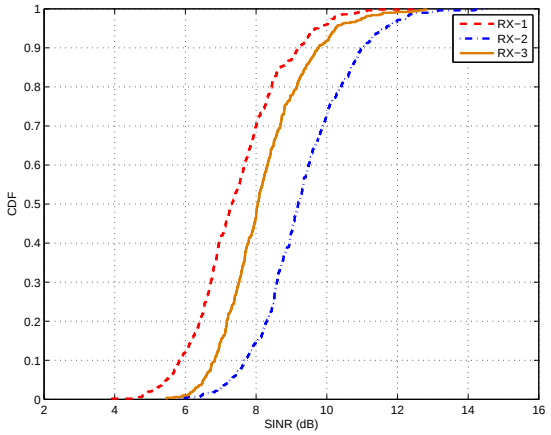

Fig. 5. SINR comparison of RX 1, RX 2 and RX 3.

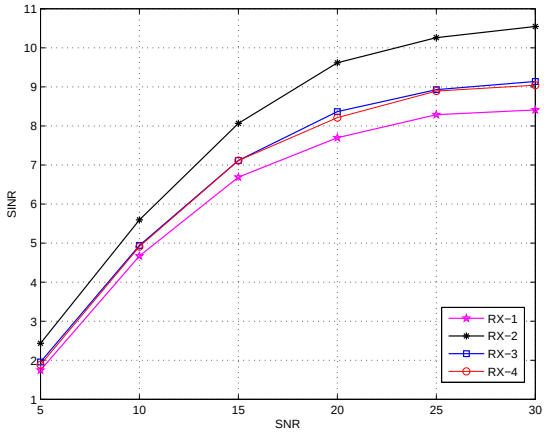

Fig. 7. SNR vs. average SINR comparison of all receivers.

channel is time-varying at the symbol level, nevertheless, we use the averaged value of the time-varying channel gain to plot the SINR. We see here that receiver-2 performs significantly better than the classical chip-equalizer correlator receiver. The complexity of the receiver-3 is significantly reduced due to the absence of inter-code interference canceling stage that is assumed present in receiver-2 but receiver-3 still outperforms receiver-1.

In Fig. 6 we compare the performance of the MRC receiver with our reference receiver. Here too we find that a receiver that first renders the channel sparse and treats the scrambler as deterministic outperforms the reference receiver. Finally in Fig. 7 we compare the performance of all receivers in terms of their average SINRs for various SNR values.

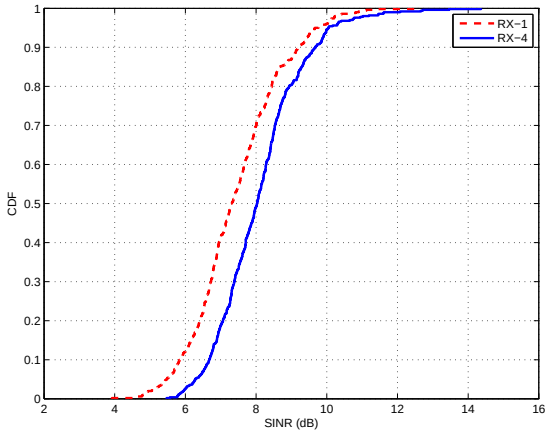

Fig. 6. SINR comparison of RX 1 and RX 4.

VI. Conclusions

In this contribution, we introduced a class of receivers for WCDMA downlink based on the novel concept of chip-level sparsification and symbol level equalization. Due to channel sparsification the resultant channel presents itself as a symbol-level ISI channel at the output of the correlator. By treating the scrambler as deterministic, the receiver can benefit from reduced parameter time-varying non-linear equalization at symbol-level. We presented solutions for obtaining the optimum channel-sparsifying filter depending on the non-linear processing stages that exploit the resultant sparse channel. We derived SINR expressions for these receivers and compared their performance against the classical MMSE chip-equalizer correlator receiver. We showed that receivers based on channel sparsification when paired with deterministic treatment of the scrambler and followed by non-linear processing stages can outperform the best chip-level linear equalization solution.

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