Optimization of Combined Chip and Symbol Level Equalization for Downlink WCDMA Reception

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Abstract— We consider iterative WCDMA receiver techniques for the UMTS FDD downlink. The popular LMMSE chip equalizer-correlator receiver does not exploit subspaces in partially loaded systems. This is in contrast to the symbol level LMMSE receiver, which is time-varying though, due to the scrambler, and hence too complex to implement. A compromise can be found by performing symbol level Multi-Stage Wiener Filtering (MSWF), which is an iterative solution in which the complexity per iteration becomes comparable to twice that of the RAKE receiver. Since the MSWF works best when the input is white, better performance is obtained if the RAKE in each MSWF stage gets replaced by a chip equalizer-correlator. One of the main contributions here is to point out that the chip equalizer benefits from a separate optimization in every stage. This is shown through a mix of analysis and simulation results.

I. INTRODUCTION

LMMSE receiver is complex for UMTS FDD mobile terminals since it not only requires inversion of a large user cross-correlation matrix but also needs the code and the amplitude knowledge of all the active users [1]. Furthermore, LMMSE solution changes every chip period due to aperiodic scrambling. The LMMSE chip equalizer-correlator is a suboptimal but much simpler alternative which is derived by modeling the scrambler as a stationary random sequence [2], [3]. Another suboptimal multiuser detector that explicitly focuses on subtracting the signals of interfering codes is the parallel interference cancellation (PIC) receiver [4]. It is well known that, under very relaxed cell loads, when the number of iterations goes to infinity, PIC might converge to the decorrelating receiver [5]. However, provided that it converges, still the convergence rate is very slow and it requires many stages to obtain a reasonable performance. This is due to the existence of high cross-correlations among users, which in fact is a consequence of the low orthogonality factor obtained initially from the usage of Rake receiver in the front-end [6], [7], [8]. In this paper, to at least guarantee the convergence in realistic loading factor situations and to increase the speed of convergence, we start the decorrelation operation, i.e. the zero forcing (ZF) symbol equalization from the output of LMMSE chip equalizer correlator front end receiver whose orthogonality factor is higher than the Rake receiver. For approximating this matrix inversion operation, we consider the polynomial expansion (PE) technique which is a better

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structured equivalent of PIC [9].

II. DOWNLINK TRANSMISSION MODEL

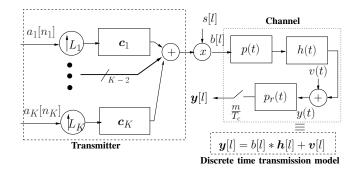


Fig. 1. Baseband UMTS downlink transmission model

The baseband downlink transmission model of the *multirate* UMTS-FDD downlink system is given in Figure 1.

At the transmitter, the K linearly modulated multi-rate user symbols with different powers are first upsampled by factors equal to their spreading factors SF- L_k where k is the user index and then convolved with their unit-energy channelization codes c_k . User symbol periods T_k and the common chip period T_c are related by $T_k = L_k \times T_c$. The sum of all the generated chip sequences is multiplied with the unit-magnitude BS-specific aperiodic scrambling sequence s[l]. The resultant BS chip sequence b[l] is transmitted to the channel which is common for all user codes since users are chip synchronous and we consider the deployment scenario where there is no beamforming. The channel is a cascade of the pulse shape filter p(t), the propagation channel h(t) and the receiver front end filter $p_r(t)$. After sampling, the overall continuous time transmission channel can be interpreted as discrete multichannels by the mobile receiver if the signal is captured by multiple sensors and/or sampled at an integer multiple of the chip rate, rendering effectively the total number of samples per chip as m > 1. Stacking these m samples in vectors, we get the received vector signal

$$\boldsymbol{y}[l] = \sum_{i=0}^{N-1} \boldsymbol{h}[i]\boldsymbol{b}[l-i] + \boldsymbol{v}[l]$$
(1)

where N is the channel length in chips, v[l] represents the intercell interference plus noise and

Although the transmission system is multirate, it can equivalently be represented as a multicode *pseudo-system* at any chosen single SF level L. When L is chosen as the highest active SF which, ignoring the very rarely used factor 512, can be taken as 256 for FDD downlink, then blocks of $256/L_k$ active symbols with SF- L_k have $256/L_k$ counterpart pseudo-symbols at SF-256. One can detect the activity or absence of pseudocodes at the pseudo-level 256 by comparing the powers at their correlator outputs with a noise-floor threshold [10]. These multiple correlations can be realized with $O(L \log L)$ complexity using Fast Walsh Hadamard Transformation (FWHT). Pseudocodes might be used in place of the unknown actual codes since the actual symbol estimates and their powers are not necessary as long as the pseudo-symbols are treated linearly in interference cancellation. However, knowing or detecting the actual codes is an opportunity for exploiting hard or hyperbolic-tangent nonlinearities or even channel decoding and encoding to refine their symbol estimates [11], [12]. In the latter case, one can pass between the symbol blocks of known codes and their pseudo-equivalents at SF-256 by properly dimensioned FWHTs. By this way hybrid treatment, i.e. respective nonlinear and linear treatment of known and unknown codes, becomes possible.

III. POLYNOMIAL EXPANSION RECEIVER

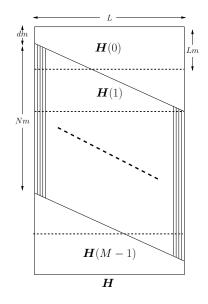


Fig. 2. Channel impulse response of H(z).

We model the discrete time received signal over one pseudosymbol period as

$$\boldsymbol{Y}[n] = \boldsymbol{H}(z)\boldsymbol{S}[n]\boldsymbol{C}\boldsymbol{A}[n] + \boldsymbol{V}[n] = \widetilde{\boldsymbol{G}}(n, z)\boldsymbol{A}[n] + \boldsymbol{V}[n]$$

representing the system at the symbol rate. As shown in Figure 2, $H(z) = \sum_{i=0}^{M-1} H[i] z^{-i}$ is the symbol rate $Lm \times L$ channel transfer function, z^{-1} being the symbol period delay operator. The block coefficients H(i) are the $M = \lfloor \frac{L+N+d-1}{L} \rfloor$ parts of the block Toeplitz matrix with $m \times 1$ sized blocks, h being the first column whose top entries might be zero for it comprises the transmission delay d between the BS and the mobile terminal. In this representation, h[0] carries the signal part corresponding to A[n] where there is no user of interest inter-symbol interference (ISI) or multi-user intersymbol interference (MU-ISI) but only user of interest interchip interference (ICI) and multi-user inter-chip interference (MU-ISI from A[n-i]. The $L \times L$ matrix S[n] is diagonal and contains the scrambler for symbol period n. The column vector A[n] contains the K (pseudo-)symbols and C is the $L \times K$ matrix of the K active codes.

Although it is possible to find an FIR left inverse filter for $\tilde{G}(n, z)$ provided that $Lm \geq K$, this is not practical since $\tilde{G}(n, z)$ is time-varying due to the aperiodicity of the scrambling. Therefore, we will introduce a less complex approximation to this inversion based on the polynomial expansion technique [9]. Instead of basing the receiver directly on the received signal, we shall first introduce a dimensionality reduction step from Lm to K by equalizing the channels with Linear Minimum Mean Square Error Zero Forcing (LMMSE-ZF) chip rate equalizers F(z) followed by a bank of correlators. LMMSE-ZF equalizer is the one among all possible ZF equalizers which minimizes the MSE at the output [13].

Let X[n] be the $K \times 1$ correlator output, which would correspond to the Rake receiver outputs if channel matched filters were used instead of channel equalizers. Then,

$$\begin{split} \boldsymbol{X}[n] &= \tilde{\boldsymbol{F}}(n,z)\boldsymbol{Y}[n] \\ &= \boldsymbol{C}^{H}\boldsymbol{S}^{H}[n]\boldsymbol{F}(z)(\tilde{\boldsymbol{G}}(n,z)\boldsymbol{A}[n] + \boldsymbol{V}[n]) \\ &= \boldsymbol{M}(n,z)\boldsymbol{A}[n] + \tilde{\boldsymbol{F}}(n,z)\boldsymbol{V}[n] \end{split}$$

where $M(n, z) = \tilde{F}(n, z)\tilde{G}(n, z)$ and ZF equalization results in F(z)H(z) = I. Hence,

$$\boldsymbol{M}(n,z) = \sum_{i=-\infty}^{\infty} \boldsymbol{M}[n,i] z^{-i} = \begin{bmatrix} \boldsymbol{I} & *\\ * & \boldsymbol{I} \end{bmatrix}$$
(3)

due to proper normalization of the code energies.

In order to obtain the estimate of A[n], we initially consider the processing of X[n] by a decorrelator as

$$\widehat{\boldsymbol{A}}[n] = \boldsymbol{M}(n, z)^{-1} \boldsymbol{X}[n]$$

$$= (\boldsymbol{I} - \overline{\boldsymbol{M}}(n, z))^{-1} \boldsymbol{X}[n].$$

$$(4)$$

The correlation matrix M(n, z) has a coefficient M[n, 0] with a dominant unit diagonal in the sense that all other elements of the M[n, i] are much smaller than one in magnitude. Hence, the polynomial expansion approach suggests to develop $(I - \overline{M}(n, z))^{-1} = \sum_{i=0}^{\infty} \overline{M}(n, z)^i$ up to some finite order, which after dropping indices leads to the iterative receiver as

$$\begin{aligned}
\mathbf{A}^{(-1)} &= 0 \; ; \; i \ge 0 \; . \\
\widehat{\mathbf{A}}^{(i)} &= \mathbf{X} + \overline{\mathbf{M}} \, \widehat{\mathbf{A}}^{(i-1)} \; , \\
&= \mathbf{X} + (\mathbf{I} - \mathbf{M}) \, \widehat{\mathbf{A}}^{(i-1)} \; , \\
&= \widehat{\mathbf{A}}^{(i-1)} + \widetilde{\mathbf{F}}^{i} (\mathbf{Y} - \widetilde{\mathbf{G}} \, \widehat{\mathbf{A}}^{(i-1)}) \; . \end{aligned}$$
(5)

The resultant receiver architecture is given in Figure 3. A practical receiver would be limited to a few orders, the quality of which depends on the degree of dominance of the static part of the diagonal of M(n, z) given in (5) with respect to its multiuser interference (MUI) carrying off-diagonal elements and the ISI carrying dynamic contents of the diagonal elements.

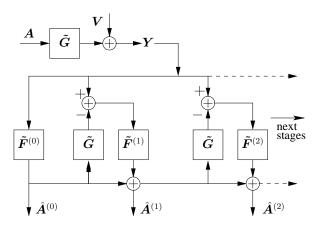


Fig. 3. Polynomial expansion receiver

In an iterative PE approach, it is advantageous to replace several *local* receiver components obtained from *global* LMMSE-ZF formulation by their LMMSE counterparts. Such modifications should lead to smaller offdiagonal power and hence faster convergence of the iterations to an estimate that is closer to a global MMSE estimate. For example LMMSE-ZF chip equalizers can be replaced by LMMSE chip equalizers which, though perturb the orthogonal structure of the received signal from the BS, do not enhance as much the intercell interference plus noise [14]. Although, due to lack of space, we do not cover those aspects in this text, the symbol estimates can also be improved in a variety of ways by symbolwise linear or nonlinear functions like LMMSE weighting factors, hard decisions, a variety of soft decisions or even channel decoding and encoding blocks.

IV. FILTER ADAPTATION

Figure 4 shows the open form of the receiver in Figure 3 where we clearly see the chip level blocks. We can further obtain a third equivalent architecture given in Figure 5 which, different from the previous two, iterates over chip estimates at chip level filter outputs. As a last simplification step, we consider the *full-cell-load* situation when all the spreading, scrambling, descrambling and despreading operations disappear, leading us to the architecture in Figure 6, which contains only chip level filters.

INITIALIZATION (First Stage) $\mathcal{X}_0 = F_0 H - I$ $\mathcal{Y}_0 = F_0$ $\tilde{B}_0 = \mathcal{X}_0 B + \mathcal{Y}_0 V$

ITERATIONS (Interference Cancellation Stages)

for
$$(i > 0)$$
 and $(i < i_{max})$
 $\boldsymbol{\mathcal{X}}_{i} = (\boldsymbol{I} - \boldsymbol{F}_{i}\boldsymbol{H})\boldsymbol{\mathcal{X}}_{i-1}$
 $\boldsymbol{\mathcal{Y}}_{i} = (\boldsymbol{I} - \boldsymbol{F}_{i}\boldsymbol{H})\boldsymbol{\mathcal{Y}}_{i-1} + \boldsymbol{F}_{i}$
 $\tilde{\boldsymbol{B}}_{i} = \boldsymbol{\mathcal{X}}_{i}\boldsymbol{B} + \boldsymbol{\mathcal{Y}}_{i}\boldsymbol{V}$
 $\arg_{\boldsymbol{F}_{i}} \min \frac{1}{2\pi j} \oint \frac{dz}{z} \left(\boldsymbol{\mathcal{X}}_{i}\boldsymbol{\mathcal{X}}_{i}^{\dagger}\sigma_{b}^{2} + \boldsymbol{\mathcal{Y}}_{i}\boldsymbol{\mathcal{Y}}_{i}^{\dagger}\sigma_{v}^{2}\right)$ (6)
 $\boldsymbol{F}_{i} = \boldsymbol{S}_{\tilde{b}_{i-1}\boldsymbol{y}_{i}}\boldsymbol{S}_{\boldsymbol{y}_{i}\boldsymbol{y}_{i}}^{-1}$
 $\boldsymbol{S}_{\tilde{b}_{i-1}\boldsymbol{y}_{i}} = \boldsymbol{\mathcal{X}}_{i-1}\boldsymbol{\mathcal{X}}_{i-1}^{\dagger}\boldsymbol{H}^{\dagger}\sigma_{b}^{2} - \boldsymbol{\mathcal{Y}}_{i-1}\left(\boldsymbol{I} - \boldsymbol{H}\boldsymbol{\mathcal{Y}}_{i-1}\right)^{\dagger}\sigma_{v}^{2}$
 $\boldsymbol{S}_{\boldsymbol{y}_{i}\boldsymbol{y}_{i}} = \boldsymbol{H}\boldsymbol{\mathcal{X}}_{i-1}\boldsymbol{\mathcal{X}}_{i-1}^{\dagger}\boldsymbol{H}^{\dagger}\sigma_{b}^{2} + (\boldsymbol{I} - \boldsymbol{H}\boldsymbol{\mathcal{Y}}_{i-1})\left(\boldsymbol{I} - \boldsymbol{H}\boldsymbol{\mathcal{Y}}_{i-1}\right)^{\dagger}\sigma_{v}^{2}$

end

The Multi-stage Wiener (LMMSE) filter adaptation procedure for the fully-loaded cell setting is given in the equations group (6) where $\left\{ \boldsymbol{\mathcal{X}}_{i}, \boldsymbol{\mathcal{Y}}_{i}, \tilde{\boldsymbol{B}}_{i} \right\}$ respectively denote {transfer function between the BS signal and the residual BS signal, transfer function for the intercell interference plus noise, residual interference plus noise} at iteration i^1 . The LMMSE optimization process output is the complete filter expression of F_i from which we derive its two ingredients $S_{\tilde{b}_{i-1}y_i}$ and $S_{y_iy_i}$ by factorization. At first sight, considering such a full load architecture seems unnecessary since LMMSE filter F_0 in the first stage is already optimal and there is no need to iterate any more. Indeed when one obtains the optimal values for $F_i, \forall i > 0$, they turn out to be all-zero vectors. However, the structure of the factorized terms are clear guidelines for understanding that the chip level filter F_i intends to estimate and subtract the residual interference plus noise term at the preceding iteration, which is also valid for more realistic partially-loaded systems with additional system components such as hard decisions. For example, if we consider the loop among the signals \hat{b}_0 , y_1 and \hat{b}_1 that contains the transfer functions $F_1(z)$ and H(z), it estimates the residual signal b_0 and subtracts it from b_0 which leads to the creation of new residual signal \tilde{b}_1 . The same reasoning holds for subsequent iterations where the amount of interference plus noise variance $\sigma_{\tilde{b}_i}^2$ is expected to decrease with increasing *i* in partially-loaded systems.

A. Adaptation for the Partial Cell Load Setting

Having understood by full load analysis what the chip level Wiener filters intend to do, we reconsider the partial

¹Each bold variable in Section IV has a (z) suffix which is dropped for brevity; † stands for z-transform para-conjugate operator meaning matched filter in the time domain

cell load architecture in Figure 5. The projection operation $S[n]CC^HS^*[n]$ complicates the situation since it is not a chip level operation, it is not convolutive and for which reason it cannot be easily integrated into the filter optimization expression in (6). Still it has two nice properties: the diagonal part is the deterministic value $C_l I$ where C_l is the effective cell loading factor and the expected value of the non-diagonal part is zero.

INITIALIZATION (First Stage)

$$egin{aligned} oldsymbol{\mathcal{X}}_0 &= oldsymbol{F}_0oldsymbol{H} - oldsymbol{I} \ oldsymbol{\mathcal{Y}}_0 &= oldsymbol{F}_0 \ oldsymbol{ ilde{B}}_0 &= oldsymbol{\mathcal{X}}_0oldsymbol{B} + oldsymbol{\mathcal{Y}}_0oldsymbol{V} \end{aligned}$$

ITERATIONS (Interference Cancellation Stages)

for
$$(i > 0)$$
 and $(i < i_{max})$
 $\boldsymbol{\mathcal{X}}_{i} = (\boldsymbol{I} - C_{l}\boldsymbol{F}_{i}\boldsymbol{H})\boldsymbol{\mathcal{X}}_{i-1}$
 $\boldsymbol{\mathcal{Y}}_{i} = (\boldsymbol{I} - C_{l}\boldsymbol{F}_{i}\boldsymbol{H})\boldsymbol{\mathcal{Y}}_{i-1} + \boldsymbol{F}_{i}$
 $\tilde{\boldsymbol{B}}_{i} = \boldsymbol{\mathcal{X}}_{i}\boldsymbol{B} + \boldsymbol{\mathcal{Y}}_{i}\boldsymbol{V}$
 $\boldsymbol{F}_{i}^{w} = \boldsymbol{S}_{\tilde{b}_{i-1}\boldsymbol{y}_{i}}\boldsymbol{S}_{\boldsymbol{y}_{i}\boldsymbol{y}_{i}}^{-1}$
 $\boldsymbol{S}_{\tilde{b}_{i-1}\boldsymbol{y}_{i}} = C_{l}\boldsymbol{\mathcal{X}}_{i-1}\boldsymbol{\mathcal{X}}_{i-1}^{\dagger}\boldsymbol{H}^{\dagger}\sigma_{b}^{2} - \boldsymbol{\mathcal{Y}}_{i-1}\left(\boldsymbol{I} - C_{l}\boldsymbol{H}\boldsymbol{\mathcal{Y}}_{i-1}\right)^{\dagger}\sigma_{v}^{2}$
 $\boldsymbol{S}_{\boldsymbol{y}_{i}\boldsymbol{y}_{i}} = C_{l}^{2}\boldsymbol{H}\boldsymbol{\mathcal{X}}_{i-1}\boldsymbol{\mathcal{X}}_{i-1}^{\dagger}\boldsymbol{H}^{\dagger}\sigma_{b}^{2} + (\boldsymbol{I} - C_{l}\boldsymbol{H}\boldsymbol{\mathcal{Y}}_{i-1})\left(\boldsymbol{I} - C_{l}\boldsymbol{H}\boldsymbol{\mathcal{Y}}_{i-1}\right)^{\dagger}\sigma_{v}^{2}$
 $\boldsymbol{F}_{i} = \frac{2\pi j \boldsymbol{F}_{i}^{w}}{\frac{dz}{z} \boldsymbol{F}_{i}^{w}\boldsymbol{H}}$: unbiasing operation (7)

end

By considering only the diagonal parts of the local projection operations, we modify the iterative scheme that we derived for the full-loading case, reaching to the expressions in equation group (7) where we also introduce the option of unbiasing. The Wiener (LMMSE) filter and unbiased LMMSE filter are denoted by F_i^w and F_i respectively.

The scheme can be modified by incorporating hard decisions this time in the context of the architecture in Figure 4 via quantifying the nonlinear SINR gain and adjusting the $S_{\tilde{b}_{i-1}y_i}$ and $S_{y_iy_i}$ which we do not cover here due to lack of space.

In practice, the approximate LMMSE filters might also be implemented as Generalized Rake (G-Rake) receivers in which case, in each stage, filtering with F_i and H will have the same complexity as a Rake receiver [15]. Hence, the filtering parts of each iteration will have twice the complexity of those of Rake.

V. SIMULATIONS AND CONCLUSIONS

For the simulations, we take a high speed packet data access (HSDPA) scenario in the UMTS-FDD downlink [16]. We consider 5 HSDPA codes at SF-16 assigned to the UE each consuming 8% of the base station power. The PCPICH pilot tone at SF-256 consumes 10% power. There is the PCCPCH code at SF-256 that consumes 4% power. To effectively model all the rest multirate user codes that we do not know, we place 46 pseudo-codes at level 256 each having 1% power.

So in total, 5 HSDSCH codes at SF-16 being equivalent to 80 pseudo-codes at SF-256, the system is effectively 50% loaded with 128 (pseudo-)codes at SF-256. Although, in practice, the pseudo-codes should be detected by a method explained in the text, for the moment, we assume that they are known. We also assume perfect knowledge of the channel. An oversampling factor of 2 and one receive antenna is used ². Static propagation channel parameters are randomly generated from the ITU Vehicular-A power delay profile. Pulse shape is the UMTSstandard, root-raised cosine with a roll-off factor of 0.22. Therefore the propagation channel, pulse shape cascade (i.e the overall channel) has a length of 19 chips at 3.84 Mchips/sec transmission rate. Symbols are QPSK. \hat{I}_{or}/I_{oc} denotes the received base station power to intercell interference plus noise power ratio. We took the average SINR result of 5 HSDPA codes over 100 realizations of one UMTS slot (160 symbol period) transmissions.

In Figure 7 we compare the performance of the PE scheme with various different chip level filter usages and iterations from one to three. The legends indicate the used filters with iteration order. For example F0-F1-F2 means optimized filters are used in different stages; F0-F0-F0 means LMMSE chip equalizer is used in all stages; F0-Rake-Rake hybrid scheme means first stage filter is LMMSE chip equalizer and subsequent two are Rake receivers; Rake-Rake-Rake corresponds to the conventional linear PIC with Rake receiver in all stages. Many other variants different from the shown ones can also be used. As is expected Rake receiver performs the worst. The conventional Linear PIC with only Rake receivers starts diverging after first iteration. This is consistent with the past literature since it is well known that, for LPIC to converge, loading factor should be lower than %17 [17]. The scheme which uses only F0 saturates after second iteration. Using Rake receivers after F0 performs very well. As expected adapting the filters at all iterations performs the best. Such a scheme obtains almost the same performance of F0-Rake-Rake in one less iteration, i.e with configuration F0-F1. At low \hat{I}_{or}/I_{oc} values which reflect the cell edge situations, the performance of first iteration is better than the second one. One might attribute this to the well-known ping-pong effect for LPIC [18].

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²The order of filtering and rechanneling operations have an impact on the noise term in case of polyphase filtering which we neglect for the moment

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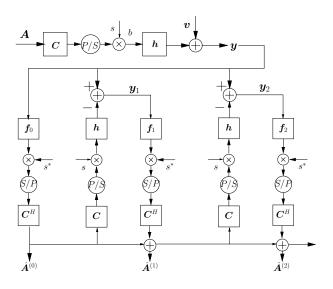


Fig. 4. Polynomial expansion receiver open format

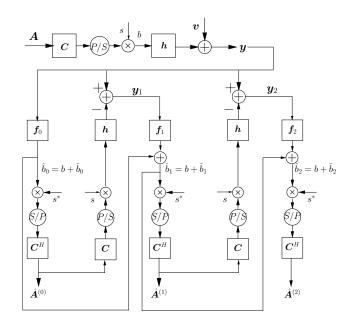


Fig. 5. PE receiver equivalent chip estimate iterating model

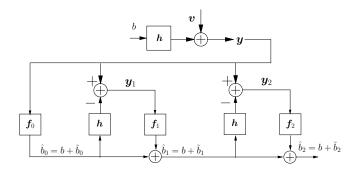


Fig. 6. PE receiver unit loading factor model

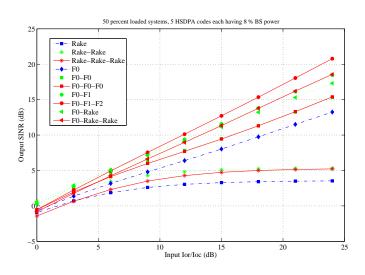


Fig. 7. SINR vs \hat{I}_{or}/I_{oc} results, Vehicular A channel, N=19